UART AUTOMATIC HALF-DUPLEX DIRECTION CONTROL WITH PROGRAMMABLE DELAY

ABSTRACT OF THE DISCLOSURE

A UART with a FIFO buffer is provided. A circuit detects a last word transmitted from the FIFO buffer. A transmitter empty circuit generates a transmitter empty signal (RTS) when the last word transmitted from the FIFO buffer is detected. A delay circuit delays generation of the RTS signal for a programmable time delay. The time delay via a register that is programmable by the user. The invention thus provides the programmable delay on the same chip as the UART.

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